CLAIMS:

1. An identification device for receiving a first signal and transmitting a second signal, the device including:

a receiving means for receiving the first signal and employing the first signal to generate a voltage;

wherein the receiving means generates a first current from the voltage;

an integrated circuit;

wherein the integrated circuit includes a state selection means for selecting whether the device is in a first state or a second state;

a connection between the receiving means and the integrated circuit;

a transmission means for generating the second signal;

wherein – relative to the second state – a relatively larger amount of the first current flows through the receiving means when the device is in the first state; and

wherein – relative to the first state – a relatively smaller amount of the first current flows through the receiving means when the device is in the second state.

2. An identification device according to claim 1 wherein:

a first probability is associated with the first state;

a second probability is associated with the second state; and

the first probability is lower than the second probability.

3. An identification device according to claim 2 wherein the first probability is at least two times lower than the second probability.

4. An identification device according to claim 2 wherein the first probability is at least four times lower than the second probability.

5. An identification device according to claim 2 wherein the first probability is at least eight times lower than the second probability.

6. An identification device according to claim 2 wherein the first probability is at least sixteen times lower than the second probability.

7. An identification device according to claim 2 wherein the relatively smaller amount of current is at least less than approximately 100 μA.

8. An identification device according to claim 7 wherein the relatively smaller amount of current is less than approximately 50 μA.

9. An identification device according to claim 8 wherein the relatively smaller amount of current is less than 30 approximately μA.

10. An identification device according to claim 9 wherein the relatively smaller amount of current is less than 15 approximately μA.

11. An identification device according to claim 10 wherein the relatively smaller amount of current is less than 5 approximately μA.

12. An identification device according to claim 11 wherein the relatively smaller amount of current is between approximately .1 μA and approximately 4.99 μA.

13. An identification device according to claim 2 wherein the relatively smaller amount of the first current is less than 50% of the relatively larger amount of the first current.

14. An identification device according to claim 13 wherein the relatively smaller amount of the first current is less than 25% of the relatively larger amount of the first current.

15. An identification device according to claim 14 wherein the relatively smaller amount of the first current is less than 5% of the relatively larger amount of the first current.

16. An identification device according to claim 15 wherein the relatively smaller amount of the first current is less than 1% of the relatively larger amount of the first current.

17. An identification device according to claim 2 wherein the first probability and second probability are at least partially random.

18. An identification device according to claim 2 wherein:

the integrated circuit has an operating cycle of a first time;

the device is in either the first state or the second state – and not both states – during the first time;

the integrated circuit receives the first signal for a second time, and

the second time is at least equal to the first time.

19. An identification device according to claim 18 wherein the second time is at least equal to the reciprocal of the first probability multiplied by the first time.

20. An identification device according to claim 2 wherein the receiving means is an antenna.

21. An identification device according to claim 20 wherein the antenna is a coil.

22. An identification device according to claim 20 wherein the receiving means is a dipole antenna.

23. An identification device according to claim 20 wherein the receiving means is a capacitive antenna.

24. An identification device according to claim 2 wherein the first signal is at least one of: an electric signal, a capacitive signal, an inductive signal, a radio signal, and a magnetic signal.

25. An identification device according to claim 2 wherein the connection includes a voltage multiplier.

26. An identification device according to claim 2 wherein the connection includes a voltage rectifier.

27. An identification device according to claim 2 wherein the transmission means is connected to, and responsive to, a series regulator.

28. An identification device according to claim 2 wherein the device further includes a first device portion that is comprised of an impedance means in series with the receiving means.

29. An identification device according to claim 28 wherein the impedance means is at least one of: an extra resistor, a capacitor, and an inductor.

30. An identification device according to claim 28 wherein the impedance means is a switched impedance.

31. An identification device according to claim 2 wherein the device further includes a second device portion that is comprised of the impedance means in series with the integrated circuit.

32. An identification device according to claim 31 wherein the impedance means is a switched impedance.

33. An identification device according to claim 2 wherein the state selection means is responsive to the first signal.

34. An identification device according to claim 33 wherein the first signal includes at least one or more first signal breaks, and the state selection means is responsive to the first signal breaks.

35. An identification device according to claim 2 wherein the device further includes a memory.

36. An identification device according to claim 35 wherein the memory includes memory space for at least one of the following information units: content information, address information, and name information.

37. An identification device according to claim 2 wherein the device has a thickness between .0mm and .5mm.

38. An identification device according to claim 2 wherein the device has a width between 10mm and 10cm, and a length between 60mm and 100mm.

39. A device according to claim 2 wherein the integrated circuit includes an onboard power source.

40. A device according to claim 2 wherein the device employs a second antenna means, that is responsive to the integrated circuit, to generate the second signal.

41. An identification device according to claim 2 wherein the receiving means is also the transmission means.

42. A device according to claim 41 wherein the transmission means is responsive to the integrated circuit for generating the second signal.

43. A device according to claim 2 wherein the state selection means includes a MOSFET transistor.

44. A system for identifying articles, the system including:

a signal generator for generating a first signal;

a plurality of articles;

a plurality of identification devices, each individual device being respectively associated with each individual article;

wherein each device includes:

a receiving means for receiving the first signal and employing the first signal to generate a voltage;

wherein the receiving means generates a first current from the voltage;

an integrated circuit;

wherein the integrated circuit includes a state selection means for selecting whether the device is in a first state or a second state;

a connection between the receiving means and the integrated circuit;

a transmission means for generating the second signal;

wherein – relative to the second state – a relatively larger amount of the first current flows through the receiving means when the device is in the first state; and

wherein – relative to the first state – a relatively smaller amount of the first current flows through the receiving means when the device is in the second state.

45. A system according to claim 44 wherein each device further includes a memory.

46. A system according to claim 45 wherein the memory includes memory space for at least one of the following information units: content information, address information, and name information.

47. A system according to claim 46 further including a sorting means that sorts the articles according to at least one of the following information units: content information, address information, and name information.

48. A system according to claim 47 wherein the plurality of devices may be placed as close as 0 cm of each other without interfering with their respective receiving means' ability to receive the first signal and their respective transmissions means' ability to generate the second signal.

49. A system according to claim 47 wherein the articles are documents.

50. A system according to claim 47 wherein the articles are parcels.

51. A system according to claim 47 wherein the articles are postaged articles including at least: letters, and packages.

52. A system according to claim 47 wherein the articles are baggage.

53. A system according to claim 47 wherein the articles are inventory–related items.

54. An identification device according to claim 44 wherein:

a first probability is associated with the first state;

a second probability is associated with the second state; and

the first probability is lower than the second probability.

55. An identification device according to claim 44 wherein the first probability is at least two times lower than the second probability.

56. An identification device according to claim 44 wherein the first probability is at least sixteen times lower than the second probability.

57. An identification device according to claim 2 wherein the state selection means is comprised of a plurality of digital circuits.

58. An identification device according to claim 57 wherein the digital circuits are comprised of one of the following: a dedicated logic circuit consisting of logic gates, a state engine consisting of logic arrays, a micro controller, and a processor.

59. An identification device according to claim 57 wherein the digital circuits are comprised of a plurality of logic arrays.

60. An identification device according to claim 59 wherein the logic arrays are controlled by a microcontroller.